

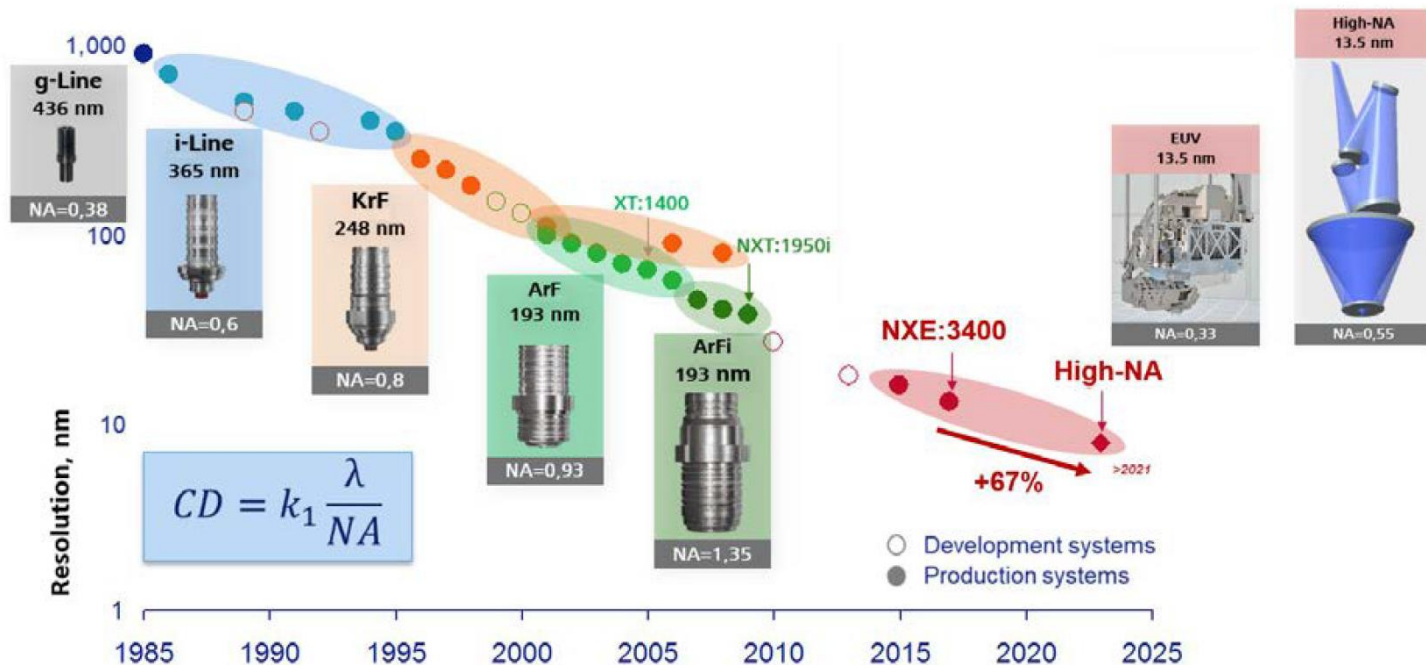


Patterning Challenges and Innovations
on the Eve of High NA EUV Lithography

Steven Scheer
SVP – Advanced Patterning Process and Materials

The lithography roadmap continues to enable scaling

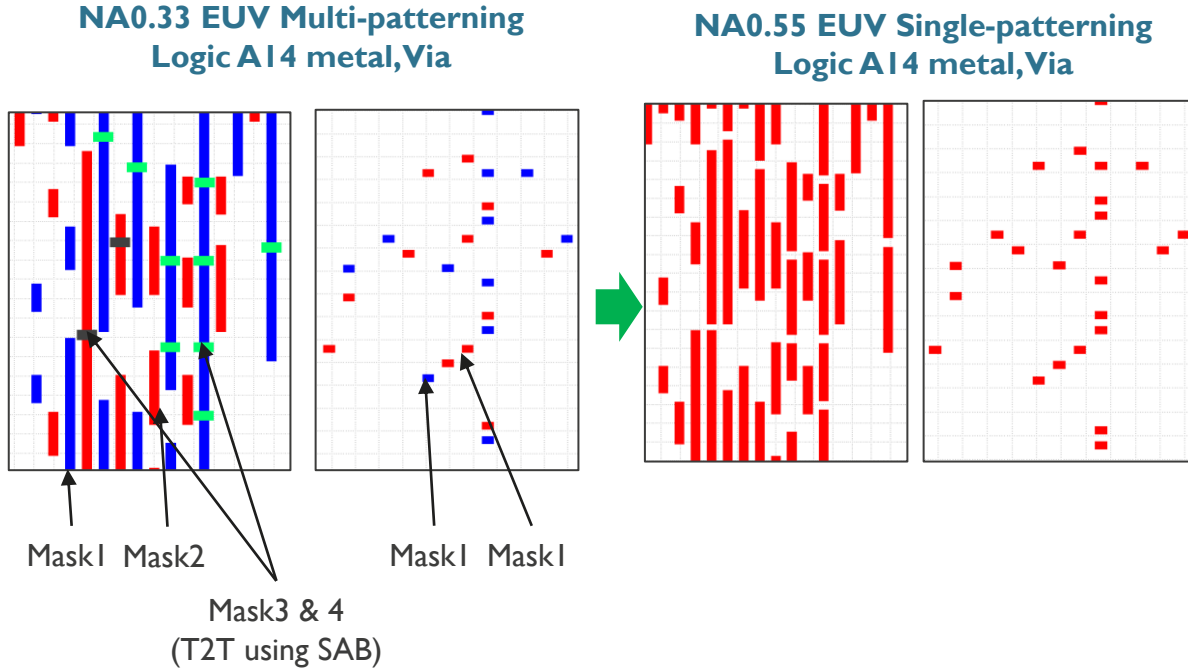
High NA EUV (0.55NA) is the next step managing complexity, turn around time and cost



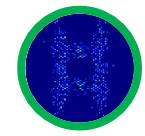
Source: Paul Graepner et al. EUV optics: status, outlook and future SPIE2022

HighNA EUV insertion scenario into LOGIC

NA0.33 EUV MPT layers' recombination into HighNA EUV single patterning use case



- **Imaging innovations needed:**
 - SMO and OPC achieving overlapping PW
- **Process innovations needed:**
 - Photoresist (thin resist)
 - Underlayer

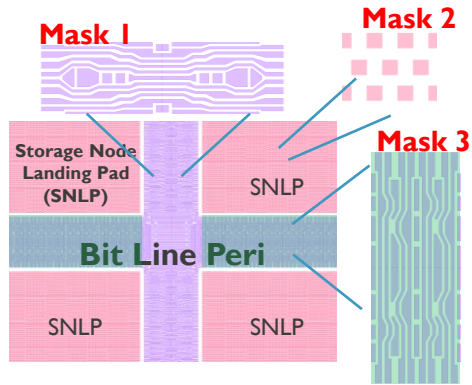


Resolution L/S + T2T and random via
Insertion at (A14) with **Extendibility (A10)**

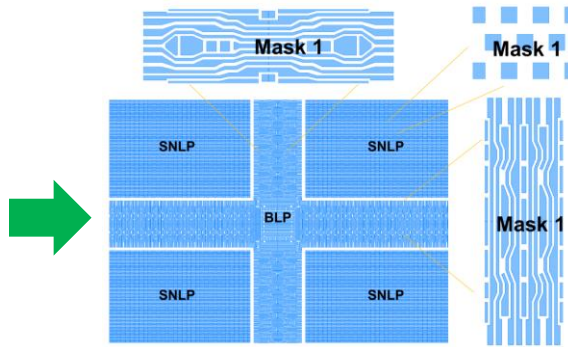
HighNA EUV insertion scenario into DRAM

NA0.33 EUV MPT layers' recombination into HighNA EUV single patterning use case

Late 10nm gen. EUV DRAM
(NA0.33 EUV multi-patterning)



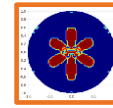
0.55NA EUV single patterning option



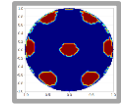
Single patterning for cost, yield,
productivity improvement

Imaging innovations needed:

- SMO and OPC achieving overlapping PW



Pitch 28



Pitch 24-25

Process innovations needed:

- Photoresist (LS + pillars)
- Pillar collapse mitigation

2D L/S with various pitches and gaps + aggressive HEX Pillars

Accelerated High NA EUV introduction via IMEC-ASML Joint High-NA LAB



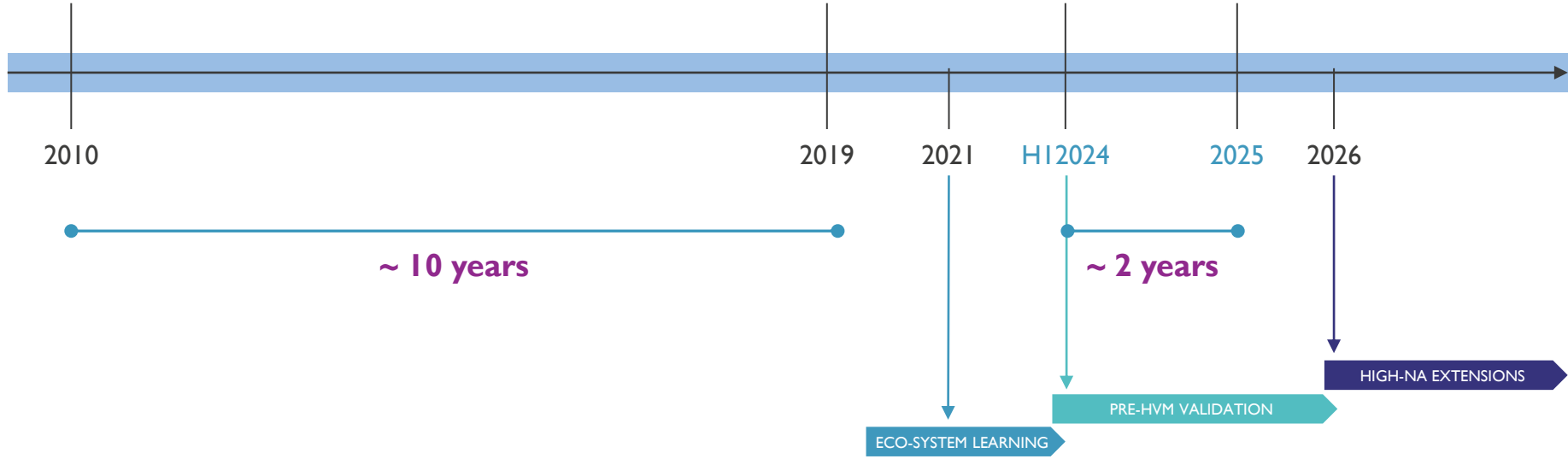
NXE3100
First prototype available



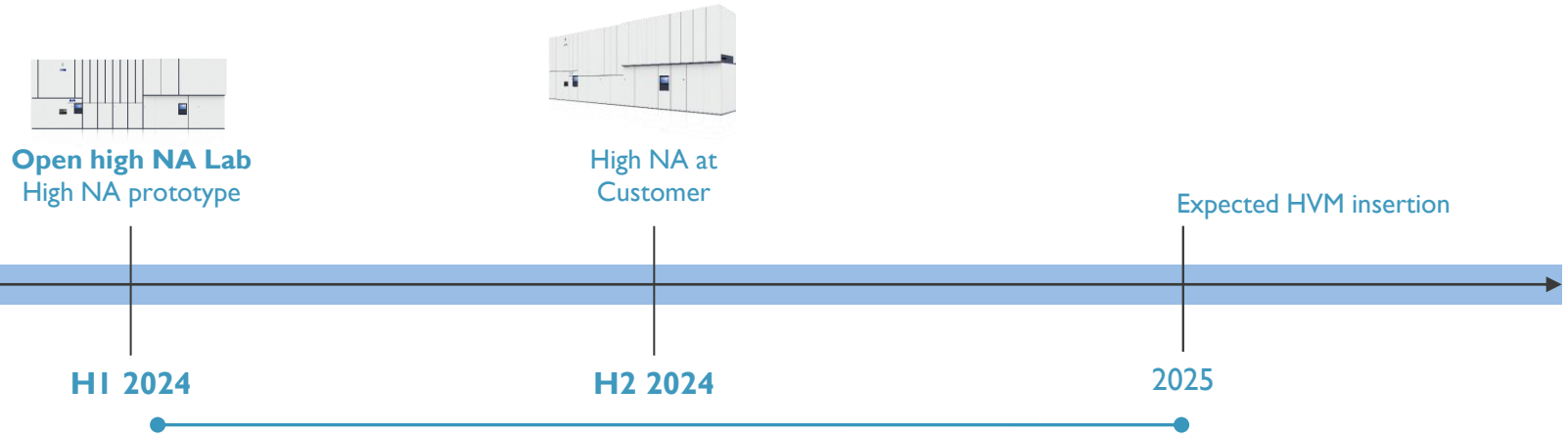
NXE3400
Actual insertion into HVM

First prototype available

Expected insertion HVM



High NA Lab enable earlier EXE access for private development and ecosystem de-risking



Objective - High NA EUV enablement and accelerated HVM insertion through:

Supporting customers' private work (development as well as technology assessment)

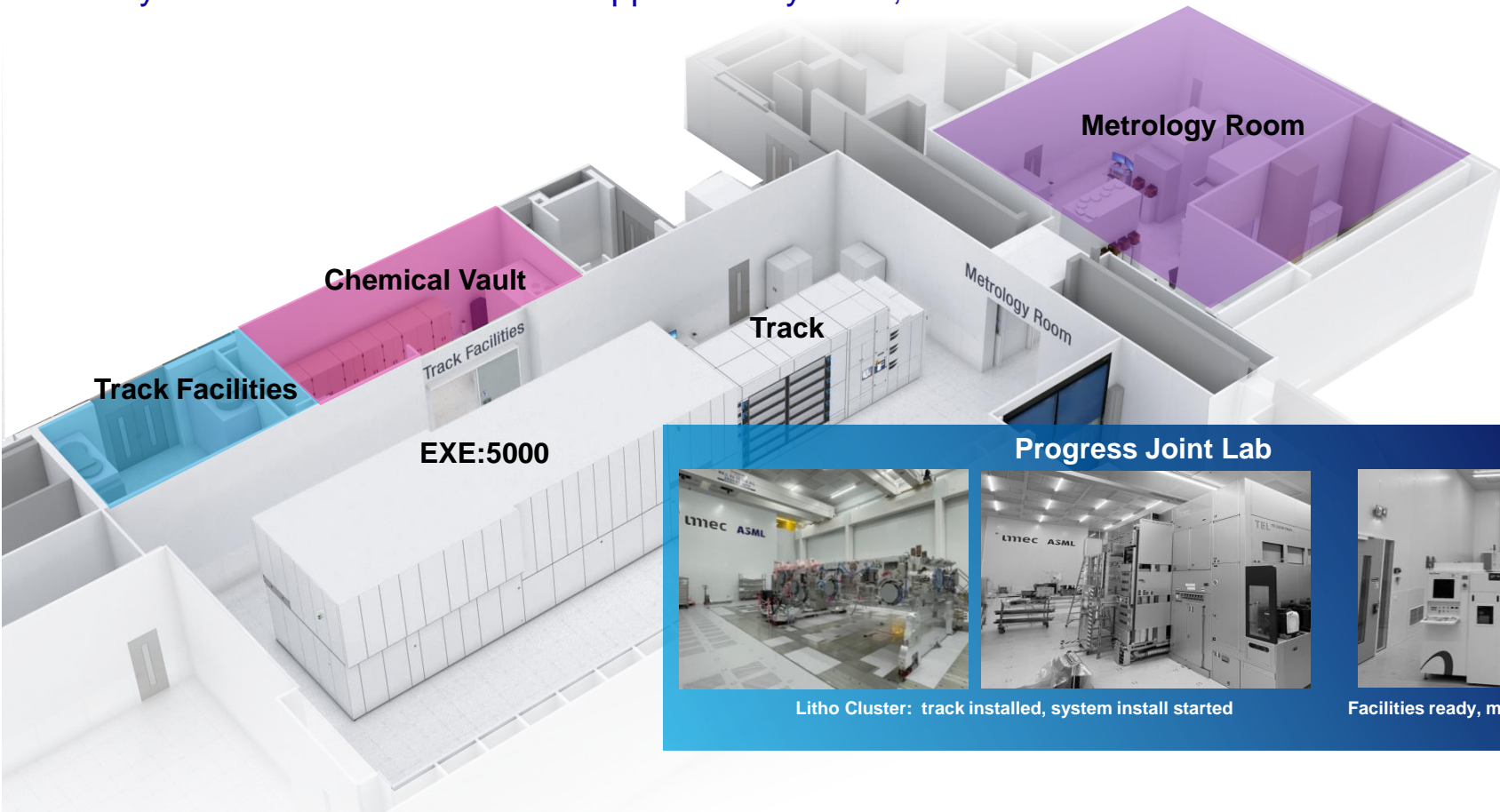
- Scanner learning, material selection, OPC, module development, ...

Securing patterning ecosystem readiness and maturity

- Understanding gaps and deliver solutions
- Leverage imec's eco-system to coordinate and enable the suppliers towards specific targets

High NA Lab offers customer access for early process development

Ready to receive customers and suppliers early 2024; EXE:5000 install started towards first image



Litho Cluster: track installed, system install started



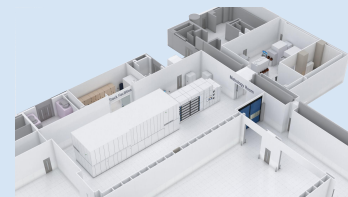
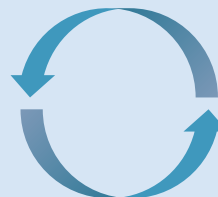
Facilities ready, metrology tools installed

imec Pilot Fab + High NA Lab – One Virtual Pilot Fab

Proximity between imec and ASML – support by imec supplier ecosystem



imec ONE VIRTUAL PILOT FAB **ASML**



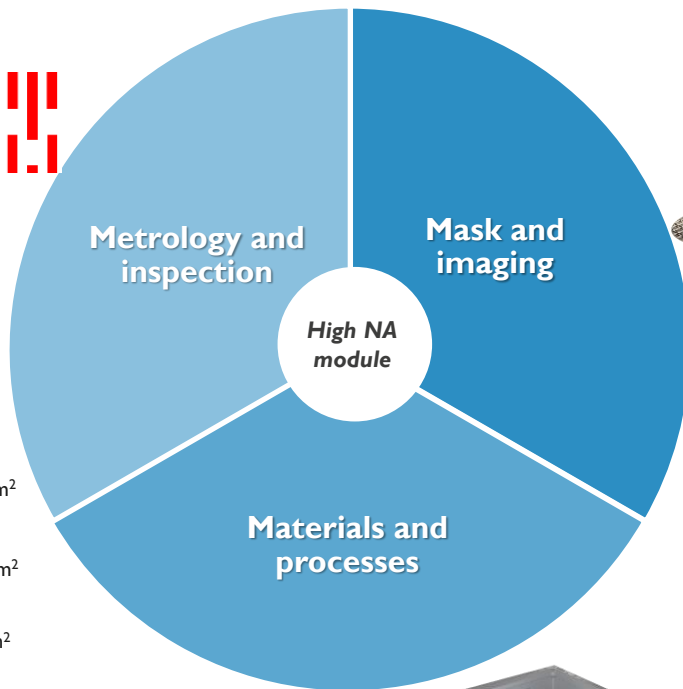
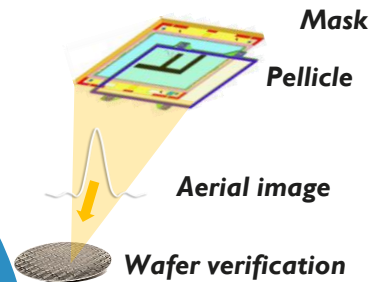
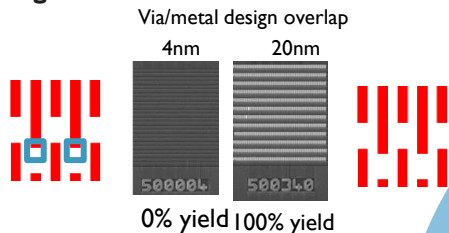
Connection to the imec ecosystem will be key to enable and ensure a timely insertion of high NA EUV technology in HVM



High NA EUV patterning module

Development focus areas

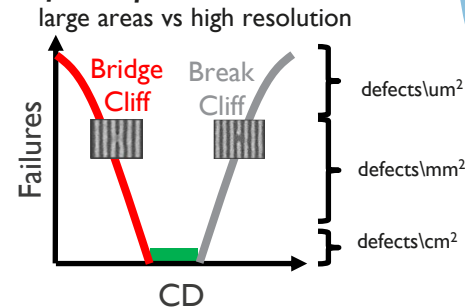
Voltage contrast



NXE3400



Defect inspection

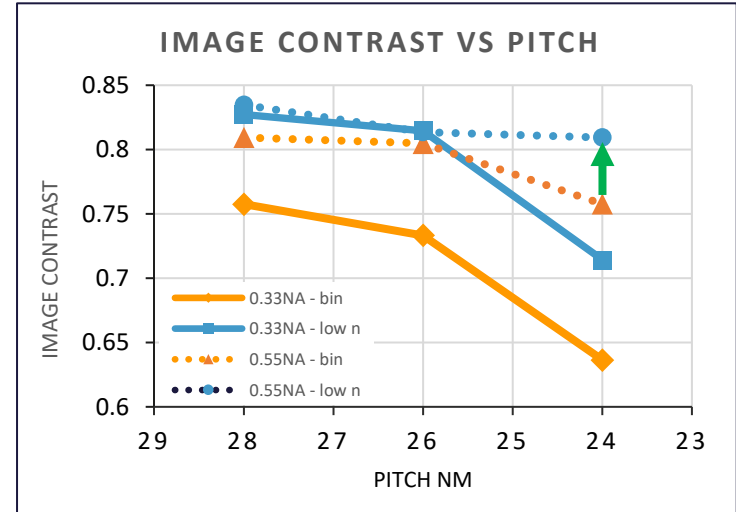
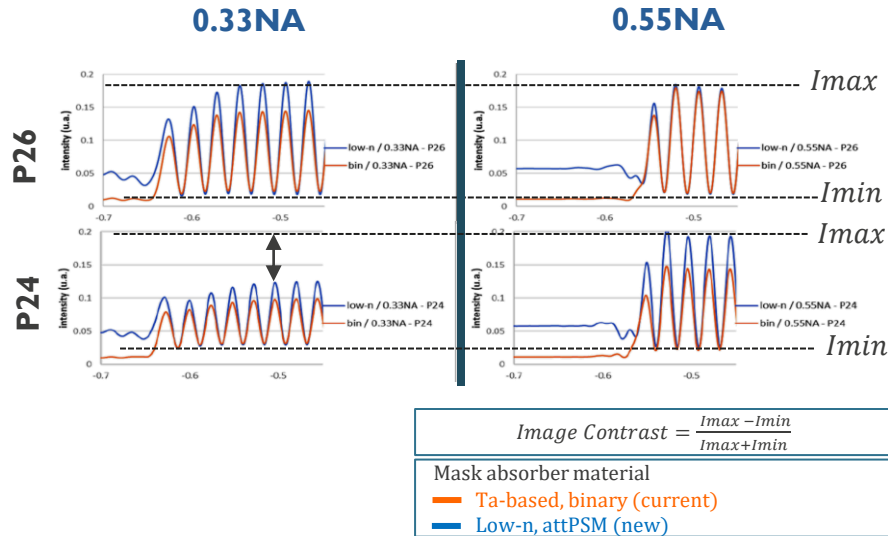
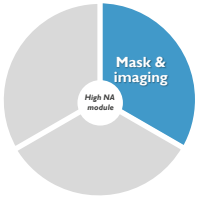


Attolab



High NA EUV patterning module

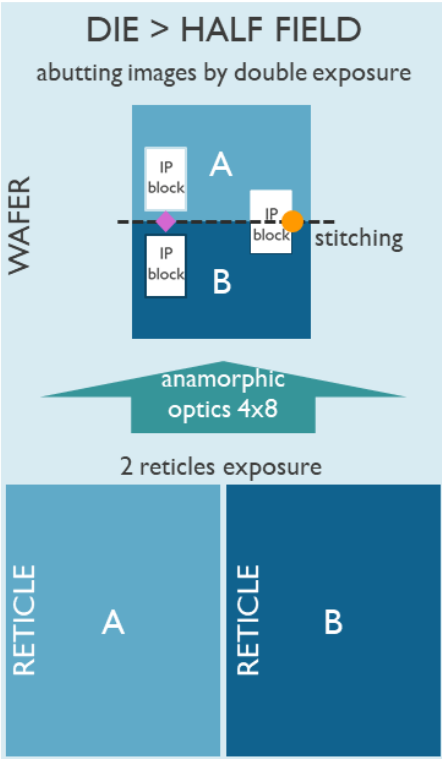
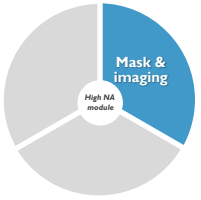
Inflection point I – mask stack: switch to **low n** absorber



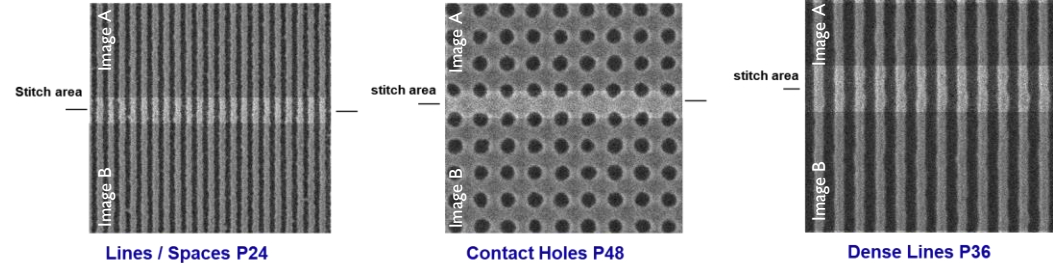
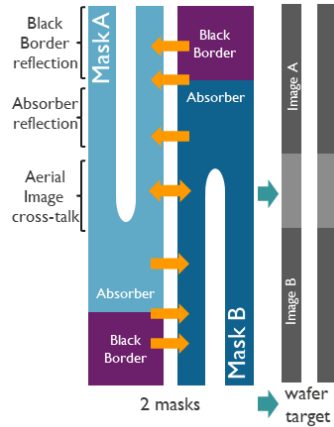
High NA EUVL needs to be complemented with mask innovation to retain high image contrast for advanced pitch scaling at pitch 24 nm LS and below

High NA EUV patterning module

Inflection point II – Anamorphic imaging and in-Die Stitching



- ◆ move IP blocks around the stitching line (ref1)
- on-resolution stitching (ref2)
 - Stitching feasibility demonstrated @NA0.33 on NXE:3400B at imec - further optimization needed

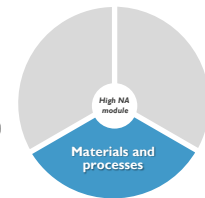


- Studying key items to enable in-die stitching
 - Optimum stitching overlap (OPC/RET, imaging, process, metrology)
 - Pattern resolution, fidelity and placement at mask in the vicinity of a black-border edge
 - Absorber to black-border transition/location
 - Low-n absorber reflectivity mitigation

Ref1: V. Wiaux EUVL2020, 11517-13; Ref2: N. Davydova EUVL2022, 12292-82 / SPIE2023, 12494-33

High NA EUV patterning module

Inflection point III – **thin photoresist** to drive the ultimate resolution (LS)



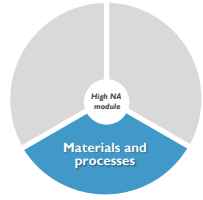
Design M2 Pitch	P32	P30	P28	P26	P24	P22	P20	P18	P17
kI at 0.33NA: Performance are imaging driven	0.39	0.37	0.34	0.32	0.29				
kI at 0.50NA (BMET5): Performance are materials driven	0.59	0.56	0.52	0.48	0.44	0.41	0.37	0.33	0.31
CAR ultimate resolution LS @ 0.5NA									
MOR ultimate resolution LS @ 0.5NA									

0.50NA (BMET)	P24	P22	P20	P18	P17
CAR FT 20nm					
MOR FT 20nm					

FT = film thickness as coated

High NA EUV patterning module

Inflection point IV – thin photoresist to drive the resolution(CH)



State of the art on NXE3400

0.33NA

pitch film thick.	P36 60nm	P34 70nm	P32 60nm
customized SMO			
Dose (mJ/cm ²)	68.5	70.5	78
LCDU (nm)	2.3	2.0	2.2
FFL (nm)	4.2	5.1	2.7

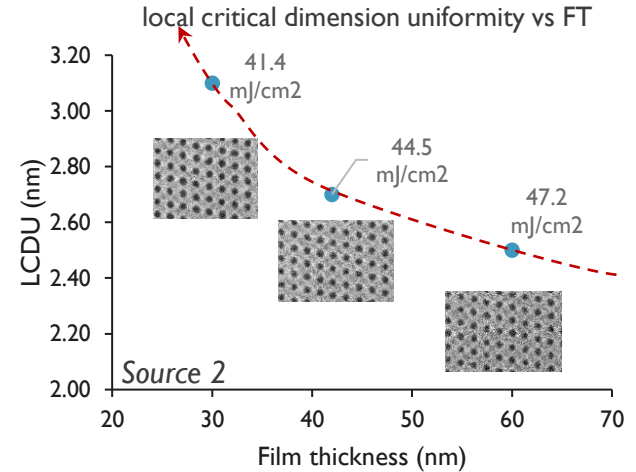
Resolution shown at 0.5NA till P26.

0.5NA BMET5

pitch film thick.	P30 60nm	P28 60nm	P26 60nm
Source 1			
Dose (BMET) (mJ/cm ²)	/	36.1	/
LCDU (nm)	NA	3.4	NA

0.5NA BMET5

P28

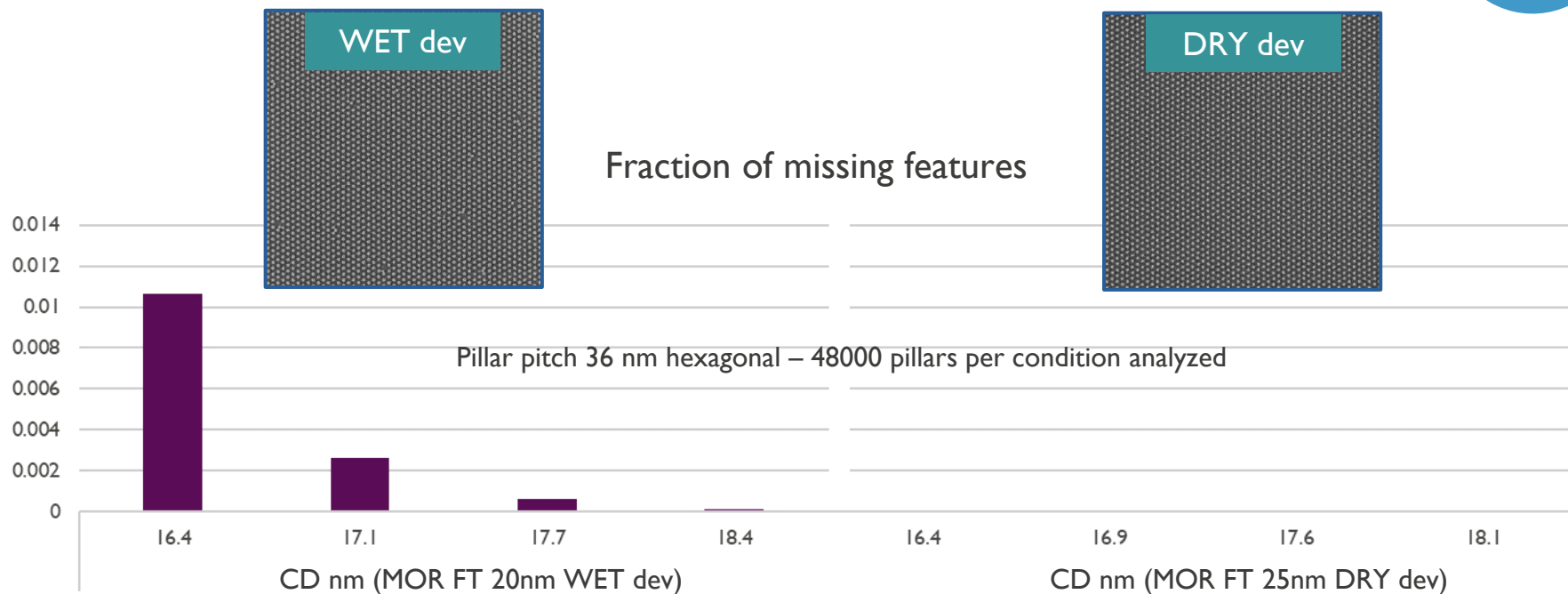
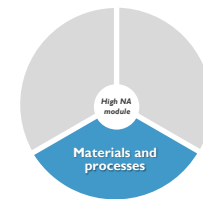


Performance improvement required for thinner resists, needs customized formulations to sustain

P28nm CH exposures at 0.5NA demonstrate that CAR can extend our DRAM roadmap beyond the point where 0.33NA starts to fail (~P30nm)

High NA EUV patterning module

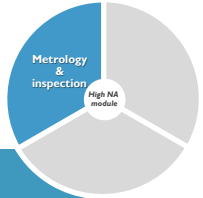
Inflection point V – development



Dry development opens pattern collapse process window at tight pitches

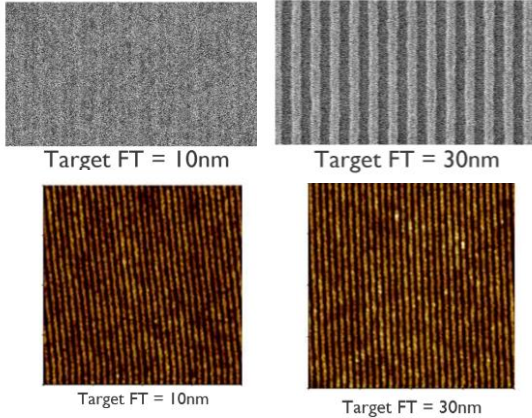
High NA EUV patterning module

Inflection point VI – Thin film resist S/N ratio



Thin resist degrade the Signal-to-Noise ratio, affecting metrology reliability and quality

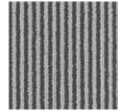
Photo resist A



Thin film metrology limited by SN ratio – imec working on material, equipment & algorithms to enable film scaling for future nodes

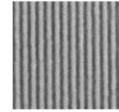
TOOLS

MOR : FT=12nm / ULI=20nm



3σ = 0.12 nm @Vacc=300V

CAR : FT=20nm / ULI=20nm



3σ = 0.13 nm @Vacc=100V

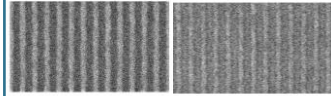
SNR improvement by landing energy optimization allows to meet high NA precision specs

MATERIAL

Photoresist A – different UL

UL1

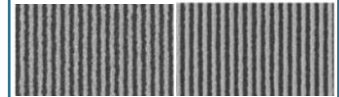
UL2



Target FT = 10 nm

Resist and UL choice can improve SNR

Different photoresist (P24nm)

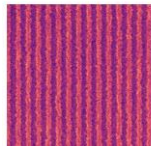


Target FT = 10 nm

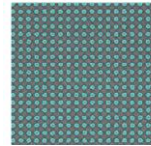
Target FT = 30 nm

ALGORITHM

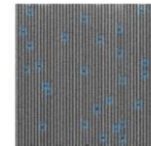
Denoiser



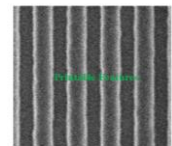
Contour Detection & Extraction



ADCD



PW Analyzer



Benefits

16X less #frames (pattern morphology unaltered)

Improving SNR (~60% enhancement)

Benefits

~150 – 200% Improved Accuracy (SIEMENS)

Layout/Design GDS not required

Benefits

~90% improved precision

Inspection time (weeks-to-hours)

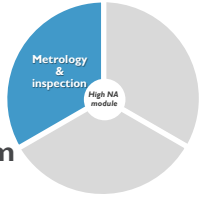
Benefits

Automated Bossung Curve analysis

Human inspection time (weeks-to-hours)

High NA EUV patterning module

Inflection point VII – optical defect inspection sensitivity

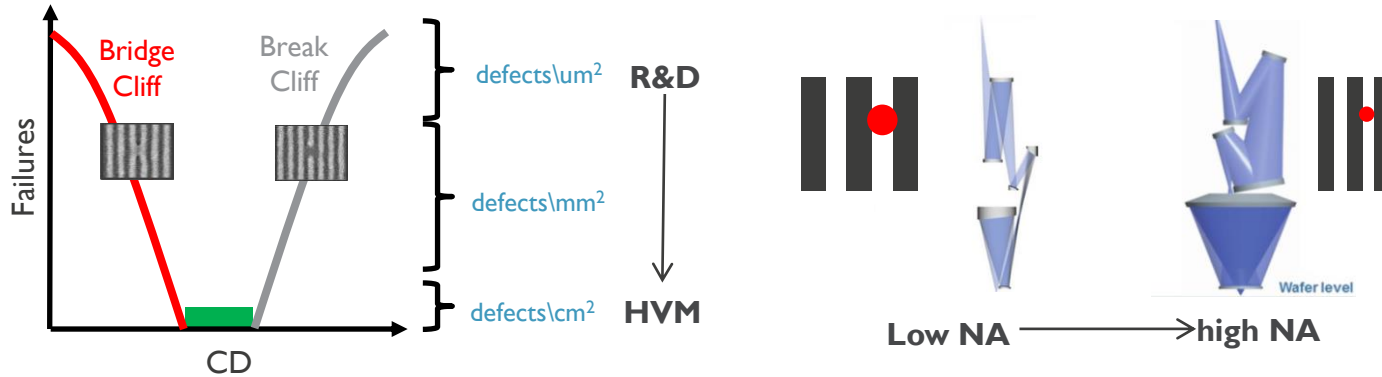


Optical E-beam



- ❑ Size Matters: Small killer defects must be detected (~1/4 pitch: 7-10nm (P28), 5-7nm (P20))
- ❑ Density Matters: Low defect density implies that large area must be detected (> 1 cm² per wafer)

The challenge is to inspect very large areas with very high resolution



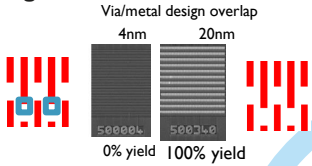
• The area requirements are related to the maturity of the process

• The size specs are related to the pitch reduction with High NA EUV

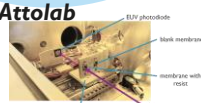
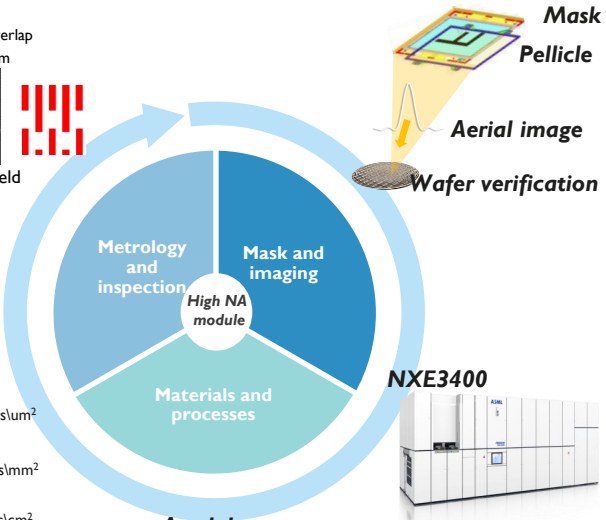
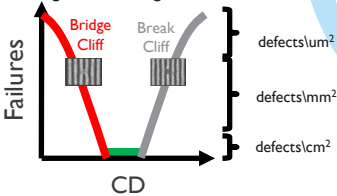
The path toward a solution is not unique yet : Broad Band Plasma, Multibeam
The imec ecosystem and demos are critical to identify an effective solution for High NA defectivity

High NA EUV – Key inflection points

Voltage contrast



Defect inspection



Mask and imaging

- **Mask absorber:** Ta based vs. low n
- **Mask tonality:** DF vs. BF
- **Anamorphic imaging:** stitching
- **OPC vs ILT:** Manhattan vs. curvilinear mask shapes
- **Pellicle:** p-Si vs. CNT

Materials and processes

- **Photoresist:** CAR vs. MOR
- **Development:** Wet vs. Dry
- **Co optimization PR/UL:** spin on vs. deposited
- **Limited resist budget** - Line break defects

Metrology and inspection

- **Defectivity:** sensitivity vs speed: optical vs. e-beam/VC
- **Resolution:** Thin film limits for LER, focus metrology
- **EPE control** : Massive CD Data volume for tail detection. Voltage contrast can simplify CH, T2T variability measurements.
- **Overlay:** intrafield overlay control in anamorphic design



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